4. (Original) A power-on reset circuit according to Claim 3, wherein said first MOS transistor is designed to be OFF when said first pulse signal is not applied thereto and to go ON with said first pulse signal applied thereto, and wherein said second MOS transistor is designed to be OFF when said second pulse signal is not applied thereto and to go ON with said second pulse signal applied thereto.

5. (Original) A power-on reset circuit according to Claim 3, wherein said timing control unit outputs said first pulse signal when the clock signal externally applied thereto is shifted from a first logical level to a second logical level, and outputs said second pulse signal when the clock signal is shifted from the second logical level to the first logical level.

6. (Original) A power-on reset circuit according to Claim 4, wherein said timing control unit outputs said first pulse signal when the clock signal externally applied thereto is shifted from a first logical level to a second logical level, and outputs said second pulse signal when the clock signal is shifted from the second logical level to the first logical level.

7. (Original) A power-on reset circuit according to any one of Claims 3, 4, 5 and 6, wherein said first capacitor is a MOS capacitor comprising a MOS transistor having its source and drain connected to said power supply line and its gate connected to said internal node.

8. (Original) A power-on reset circuit according to any one of Claims 1 to 6, wherein said output portion has a hysteresis characteristic.

9. (Original) A power-on reset circuit according to Claim 7, wherein said output portion has a hysteresis characteristic.